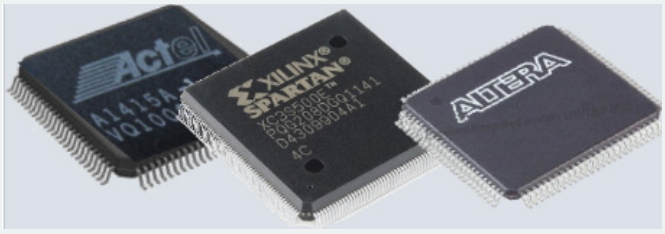
SRI International®

AME GEM

# Mitigating FPGA Obsolescence Using The Microcircuit Emulation Solution

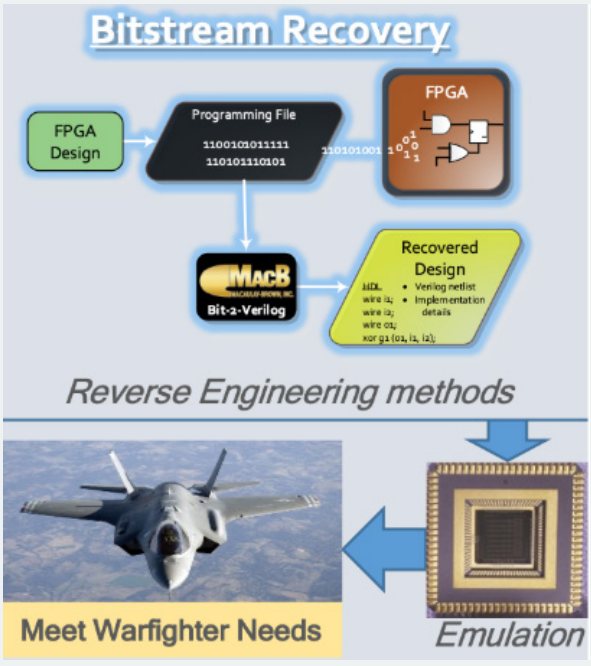
## THE NEED

Field Programmable Gate Arrays (FPGAs) are widely used throughout the defense industry as a critical component in systems. These components are user programmable, allowing the engineers to program in a design tailored to the functionality of a specific board or system. These devices can support complex designs and interface with other components through various I/O standards. FPGAs also give the designers flexibility in the event of a unique requirement or unexpected design changes.




Emulation Technology
Voltage: 3.3 V to 5.0 V
Up to 1 Million Gates
Over 200 I/O Pins
Operation: Complex Digital Functions
Target: Multiple FPGA Families

As technology advances, older FPGAs become obsolete as faster and more advanced device families are introduced. However, there are still military systems in the field that require replacement parts for these obsolete FPGAs. While FPGA vendors may recommend using a newer FPGA to replace ones that are going obsolete, they are not a suitable replacement for existing board designs as they are not Form-Fit-Function-Interface (F3I) compatible.




## THE EMULATION SOLUTION

The Defense Logistics Agency (DLA) Advanced Microcircuit Emulation (AME) program has developed a flow to Emulate FPGAs as Application Specific Integrated Circuits (ASICs). This involves taking the exact design implemented on the FPGA and targeting it to one of the Emulation gate arrays to produce an ASIC form of the design. The resulting part is not reprogrammable, but it will otherwise be form-fit-functionally equivalent to the device as programmed for use in a specific system location.

One difficulty in Emulating FPGAs is that the customer often does not have all the design information needed to reproduce the part, and the only piece of information available is the programming file used to configure the FPGA and/or PROM. Therefore, we have established a flow utilizing the reverse engineering capabilities of Macaulay-Brown, Inc. to take an FPGA programming file and/or PROM, and extract the design information (source code or netlist). Macaulay-Brown, Inc. (an Alion company) has developed the capability to do this for several generic FPGA families. including embedded memories and math blocks. These macrocells will be implemented in the converted netlist during synthesis. Once the netlist conversion is complete, the design is run through several tools to insert testing capabilities and perform place and route. The final post route design is analyzed to verify timing and functionality before it is released to fabrication.

To verify the functionality and characteristics of the final part against the original FPGA device, test boards are designed for each of the components so that they can be tested using the Automated Test Equipment (ATE). The test team has developed a flow to convert simulation waveforms into test vectors that can then be applied to the devices. This will be essential for FPGA designs as they have more complex functionality that will need to be exercised. The test engineers can run the functional test vectors on both the ASIC and FPGA to verify that the designs are functionally equivalent and meet the required specifications before delivering to the customer.

When a netlist is extracted, it can then be targeted to one of the Emulation technologies. To help with the conversion, we developed a library of macrocell components that are common among FPGAs including embedded memories and math blocks. These macrocells will be implemented in the converted netlist during synthesis. Once the netlist conversion is complete, the design is run through several tools to insert testing capabilities and perform place and route. The final post route design is analyzed to verify timing and functionality before it is released to fabrication.

## BENEFITS

The FPGA Emulation solution provides a permanent source for Form-Fit-Function-Interface (F3I) programmed FPGA-equivalent components for use in Military systems. Our FPGA to ASIC design-porting strategy is a proven method to support the Warfighter. Microcircuit Emulation is a cost-effective, long-term solution that provides total life cycle support for weapons systems, averting mission-impaired-capability-awaiting-parts (MICAP) incidence, production shutdowns, and maintaining weapon system readiness levels.

## Our Story

In the late 1980's, DLA recognized that microcircuit obsolescence threatened the readiness of many American defense systems. Numerous systems in the armed forces were designed and developed in the 1960's and 1970's. For example, the U.S. Air Force began flying the F-15 Eagle tactical fighter in 1972, and the U.S. Navy first tested the Aegis phased-array radar at sea in 1973. Because of continued advancements in semiconductor technology, the original suppliers stopped manufacturing the microelectronic components used in these and other systems. In 1987, DLA contracted with SRI to begin research and development on how to best replace obsolete microcircuits with standardized, modern integrated circuits (IC). DLA and SRI collaborated to develop the GEM Program. Using its on-site Trusted semiconductor foundry and deep knowledge of IC design/development, SRI produces on-demand, Class Q microcircuits matching the Form-Fit-Function-Interface (F3I) criteria of the required microcircuit. DLA is developing the next generation of F3I microcircuit Emulation capability through the AME Program to further alleviate growing IC obsolescence issues caused by the continued rapid advancements in technology. The new capabilities developed by AME are utilized by the GEM Program to ensure the Emulation Programs continue to meet weapons systems wide-ranging requirements. SRI's semiconductor foundry is accredited as a Department of Defense (DoD) Trusted Foundry supplier, and our manufacturing processes are qualified to MIL-PRF-38535.