Wafer Acceptance Test (WAT) and Wafer Level Reliability (WLR)

As a MIL-PRF-38535 QML certified process, Wafer Acceptance Testing (WAT) of parametric devices is used to validate that every wafer conforms to the required limits of transistor characteristics and other critical device electrical parameters. This test is used to assure the wafer was processed correctly. If the wafer meets all device specifications it is sent to wafer sort testing.

Samples from each circuit family are periodically chosen for Wafer Level Reliability (WLR) testing. WLR is a suite of accelerated tests performed at the wafer level to predict the long-term performance of the parts produced on the wafer. The tests are performed on special arrays of test devices, allowing characterization of the wafer without harm to the actual circuits. The suite consists of three types of testing:

1. Hot Carrier Injection (HCI) tests
2. Electromigration (EM) tests
3. Oxide integrity tests

HCI testing runs transistors at elevated voltages, samples the device at prescribed intervals, and measures the change in a particular device parameter, e.g., threshold voltage. This is done for many transistors over a range of voltages to gather a statistically valid sample from which the transistor lifetime can be extrapolated. EM testing uses voltage and current to induce self-heating of metal lines and contacts. The elevated temperature and voltage cause changes in resistance, and lifetime is extrapolated from many samples stressed at varying temperatures. Oxide integrity stresses a gate oxide to failure by ramping the voltage and recording the voltage, current, and accumulated charge at breakdown. The minimum acceptable value for each parameter has been identified by extensive prior testing and is part of the pass/fail specification.

Wafer sort testing is done as required to reject any die which may contain a defect prior to assembly into the final package. This testing includes both functional operation and part-specific parametric screening tests (probing) of the application circuits. Wafer maps are generated based on probing results for feedback to process engineering for continuous improvement and yield enhancement.
Our Story

In the late 1980’s, DLA recognized that microcircuit obsolescence threatened the readiness of many American defense systems. Numerous systems in the armed forces were designed and developed in the 1960’s and 1970’s. For example, the U.S. Air Force began flying the F-15 Eagle tactical fighter in 1972, and the U.S. Navy first tested the Aegis phased-array radar at sea in 1973. Because of continued advancements in semiconductor technology, the original suppliers stopped manufacturing the microelectronic components used in these and other systems. In 1987, DLA contracted with SRI to begin research and development on how to best replace obsolete microcircuits with standardized, modern integrated circuits (IC). DLA and SRI collaborated to develop the GEM Program. Using its on-site Trusted semiconductor foundry and deep knowledge of IC design development, SRI produces on-demand, Class Q microcircuits matching the Form-Fit-Function-Interface (F3I) criteria of the required microcircuit. DLA is developing the next generation of F3I microcircuit Emulation capability through the AME Program to further alleviate growing IC obsolescence issues caused by the continued rapid advancements in technology. The new capabilities developed by AME are utilized by the GEM Program to ensure the Emulation Programs continue to meet weapons systems wide-ranging requirements. SRI’s semiconductor foundry is accredited as a Department of Defense (DoD) Trusted Foundry supplier, and our manufacturing processes are qualified to MIL-PRF-38535.

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