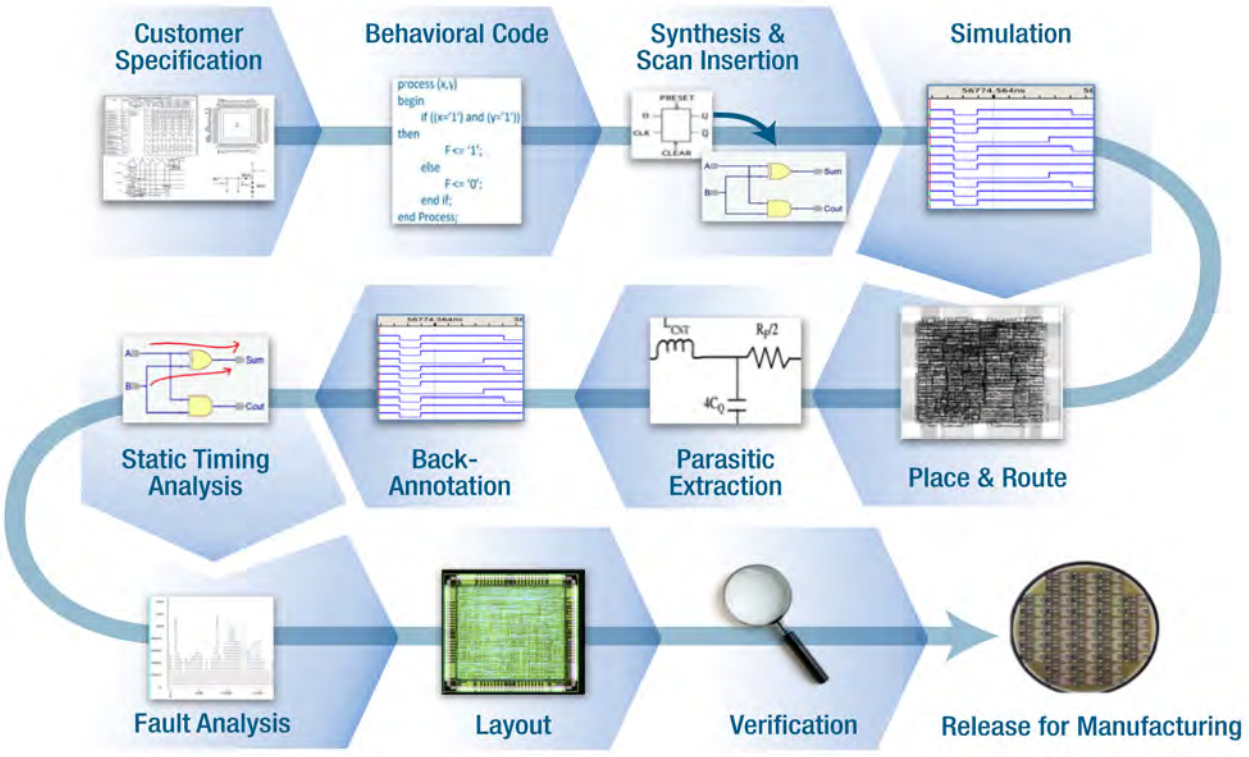
# DEFENSE LOGISTICS AGENCY
## GEM & AME PROGRAMS

# Microcircuit Emulation Design & Layout

The Microcircuit Emulation Center (MEC) integrated circuit (IC) design & layout group has provided custom circuit solutions for over 35 years in support of the Defense Logistics Agency (DLA) Generalized Emulation of Microcircuits (GEM) and Advanced Microcircuit Emulation (AME) programs. The QML-certified center maintains a Quality Management Plan to conform to the requirements of MIL-PRF-38535 and MIL-STD-883 for all aspects of circuit design, layout validation, and verification.

The design & layout group uses a state-of-the-art suite of Electronic Design Automation (EDA) tools to design Digital and Analog ICs on all the processes currently available from the Wafer Foundry as well as any future process developments. The devices in all the production processes are completely modeled to ensure the manufactured design is functionally correct and will be in full conformance with customer specifications. The design libraries for each process are characterized over the full military voltage and temperature ranges.

The design & layout group has experience designing Digital and Analog ICs. The current production processes provide the capability to design circuits with a dozen bipolar transistors through advanced complex microcircuits with millions of NMOS and PMOS transistors. The design flow can handle the synthesis and mapping of any combination of in-house and externally generated logic cores onto our processes. Layout of the designs are performed either by hand or by using advanced place & route tools. The parasitic capacitance and resistance of the back-end-of-line (BEOL) process is characterized to create back annotated netlists to verify the IC will perform to specification when manufactured. Our capability to design Op Amps, comparators and regulators up to 40 V leverages recent process developments and will be further extended to cover higher voltage Analog ICs.



## EDA Capabilities:

◆Electronic Design Automation (EDA) Tools ◆Technology Device Modeling ◆Library Characterization ◆Synthesis ◆Scan Insertion ◆Simulation ◆Static Timing Analysis ◆Fault Analysis ◆Back Annotation ◆Manual Layout Implementation ◆Place & Route ◆In-house Digital & Analog Design ◆Experienced Design & Layout Team ◆CUI Design Network Cluster

| Design: |
|---|
| Netlist development and simulation |
| Schematic capture |
| SPICE simulation |
| Behavioral simulation |
| Synthesis |
| Static timing analysis |

| Design: |
|---|
| Cell characterization |
| Fault coverage vector generation |
| Fault coverage analysis |
| Design-for-test (DFT) |
| Formal Equivalence Check |

| Layout: |
|---|
| Place and route |
| Layout capture |
| Layout verification LVS/DRC/ERC |
| DRC Deck Generation |
| Interconnect parasitic extraction |
| IR/Thermal/Power/EM Analysis |

The DLA Emulation programs maintain a Controlled Unclassified Information (CUI) compliant network cluster of Linux workstations and servers to support high uptime and availability of EDA software and data. All data are backed up daily and off-site storage is used to guard against data loss. The EDA software is regularly updated and expanded as new processes, technologies, and capabilities become available.

The MEC Design Center works closely with our on-site Trusted foundry and uses advanced TCAD tools to analyze the fabrication process. Our digital and analog design capability covers a range of technologies (CMOS, BiCMOS, Bipolar) and feature sizes, from 3.0 µm down to 0.35 µm. Our current development thrust is to add 40 V Analog capability.

## Our Story

In the late 1980s, DLA recognized that microcircuit obsolescence threatened the readiness of many American defense systems. Numerous systems in the armed forces were designed and developed in the 1960s and 1970s. For example, the U.S. Air Force began flying the F-15 Eagle tactical fighter in 1972, and the U.S. Navy first tested the AEGIS phased-array radar at sea in 1973. Because of continued advancements in semiconductor technology, the original suppliers stopped manufacturing the microelectronic components used in these and other systems. In 1987, DLA contracted with SRI to begin research and development on how to best replace obsolete microcircuits with standardized, modern integrated circuits (IC). DLA and SRI collaborated to develop the GEM Program. Using its on-site Trusted semiconductor foundry and deep knowledge of IC design/development, SRI produces on-demand, Class Q microcircuits matching the Form-Fit-Function-Interface (F3I) criteria of the required microcircuit. DLA is developing the next generation of F3I microcircuit Emulation capability through the AME Program to further alleviate growing IC obsolescence issues caused by the continued rapid advancements in technology. The new capabilities developed by AME are utilized by the GEM Program to ensure the Emulation Programs continue to meet weapons systems wide-ranging requirements. SRI's semiconductor foundry is accredited as a Department of War (DOW) Trusted Foundry supplier, and our manufacturing processes are qualified to MIL-PRF-38535.