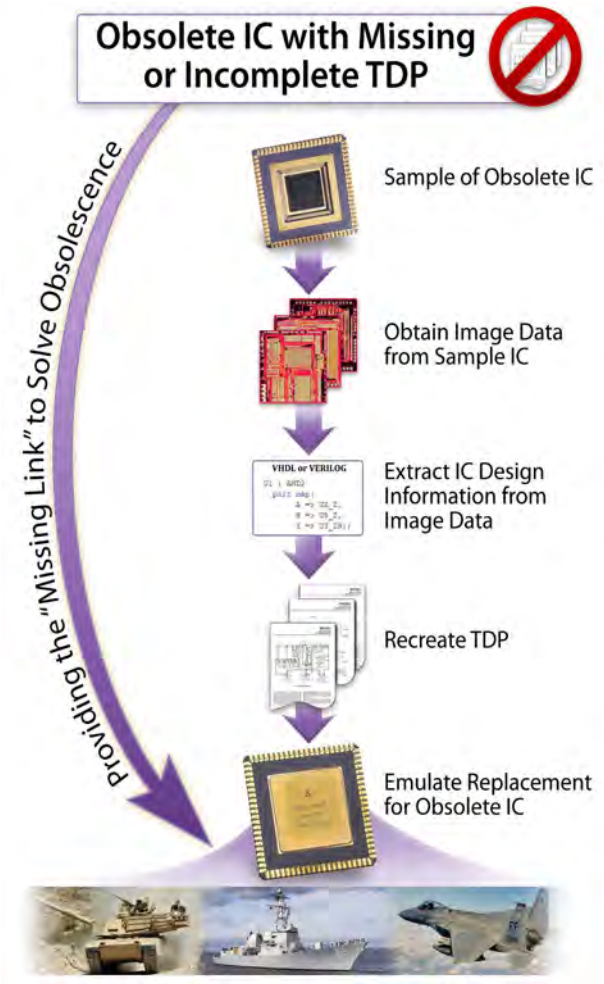
DEFENSE LOGISTICS AGENCY
GEM & AME PROGRAMS

Microcircuit Emulation Reverse Engineering

Department of War (DoW) solutions for obsolete microcircuits, particularly custom Application Specific Integrated Circuits (ASICs), are often challenging due to the Technical Data Package (TDP) being unavailable or incomplete. Even where documentation exists, it seldom contains the detailed information necessary to ensure a first-pass redesign success. In many cases, the only existing "data" is the packaged integrated circuit (IC). The Emulation process begins with "reverse engineering" (RE) the original device. This includes reviewing any existing documentation, electrical probing of the original circuit (Electrical RE), and physically inspecting the original part through careful delayering and high-resolution imaging (Physical RE).



DOCUMENT REVIEW

Document reviews include a thorough review of the detailed Government documents (Standard Military Drawing or slash sheet) or customer's component specification (e.g. Source Control Drawing) in addition to the original manufacturer's published data.

PHYSICAL REVERSE ENGINEERING

We have developed and demonstrated a physical reverse engineering capability for complex ICs. This reverse engineering process involves removing the silicon die from the package and carefully "deprocessing" the microcircuit layer-by-layer and capturing each circuit layer with optical and electron-beam microscopy. Image data is collected to extract the original design information to manufacture the microcircuit. We have the capability to derive netlists, schematics, and higher order design information directly from silicon die without additional technical data. The emulation design can then be created using GEM/AME technology and design libraries.

ELECTRICAL REVERSE ENGINEERING

A known good, sample part is electrically tested both functionally and for every specified electrical parameter using sophisticated Automatic Test Equipment (ATE) or traditional bench-top instrumentation when required. Any ambiguities may require additional tests as specified by design engineering.

The resulting measurements of this original device are reviewed relative to the specification requirements and used as a baseline for the detailed design of the emulation circuit.

ELECTRICAL TESTING CAPABILITIES

Digital ATE	Capability to test from -40 V up to 80 V Bipolar and CMOS based ICs: • Logic Families: TTL multiple generations, ECL. • Memories: Static RAM, Read Only Memories (ROM). • Programmable Devices: PLAs, PLDs, FPGAs, etc. • Digital LSI: Large pin count Microprocessors. • Microcontrollers, and ASICs.
Analog ATE	Capability to test up to 180 V linear ICs: Operational Amplifiers, Comparators, Voltages, Muxes, Regulators, and References.
Bench Testing	Combination of manual and semi-automated test routines to characterize non-trivial functional or performance parameters.
Other	ESD and Latchup characterization.
Environmental Conditioning & Testing	-55 °C to +125 °C temperature conditioning and control at DUT used on both ATE and bench tests. Tested at room temperature, -55 °C and +125°C.
Sample Preparation	• Mechanical and chemical delid/decapsulation to remove packaging • Ion mill for delayering • Reactive Ion Etching (RIE) for selective delayering • Mechanical polishing for planarization layer removal • Wet chemical delayering and dopant staining
Imaging Equipment	• Automated optical stitching microscope • Automated scanning electron microscope (SEM) • Analytical SEM with Energy Dispersive x-ray analysis (EDX) • Confocal microscope

ENSURING COMPLIANCE

The procedures developed in the Microcircuit Emulation programs provide accurate and efficient reverse engineering ensuring microcircuit conformance with all specifications within procurement documents. The GEM program supports the Warfighter and provides a long term supply of obsolete microcircuits to DoD systems.

Our Story

In the late 1980s, DLA recognized that microcircuit obsolescence threatened the readiness of many American defense systems. Numerous systems in the armed forces were designed and developed in the 1960s and 1970s. For example, the U.S. Air Force began flying the F-15 Eagle tactical fighter in 1972, and the U.S. Navy first tested the AEGIS phased-array radar at sea in 1973. Because of continued advancements in semiconductor technology, the original suppliers stopped manufacturing the microelectronic components used in these and other systems. In 1987, DLA contracted with SRI to begin research and development on how to best replace obsolete microcircuits with standardized, modern integrated circuits (IC). DLA and SRI collaborated to develop the GEM Program. Using its on-site Trusted semiconductor foundry and deep knowledge of IC design/development, SRI produces on-demand, Class Q microcircuits matching the Form-Fit-Function-Interface (F3I) criteria of the required microcircuit. DLA is developing the next generation of F3I microcircuit Emulation capability through the AME Program to further alleviate growing IC obsolescence issues caused by the continued rapid advancements in technology. The new capabilities developed by AME are utilized by the GEM Program to ensure the Emulation Programs continue to meet weapons systems wide-ranging requirements. SRI's semiconductor foundry is accredited as a Department of War (DOW) Trusted Foundry supplier, and our manufacturing processes are qualified to MIL-PRF-38535.